

# MEMORY DEVICE HAVING REDUNDANT MEMORY CELL

Application No. NEW - Attorney Docket No. OKI.650

Inventor: Tatsuya TANABE

101: DRAM

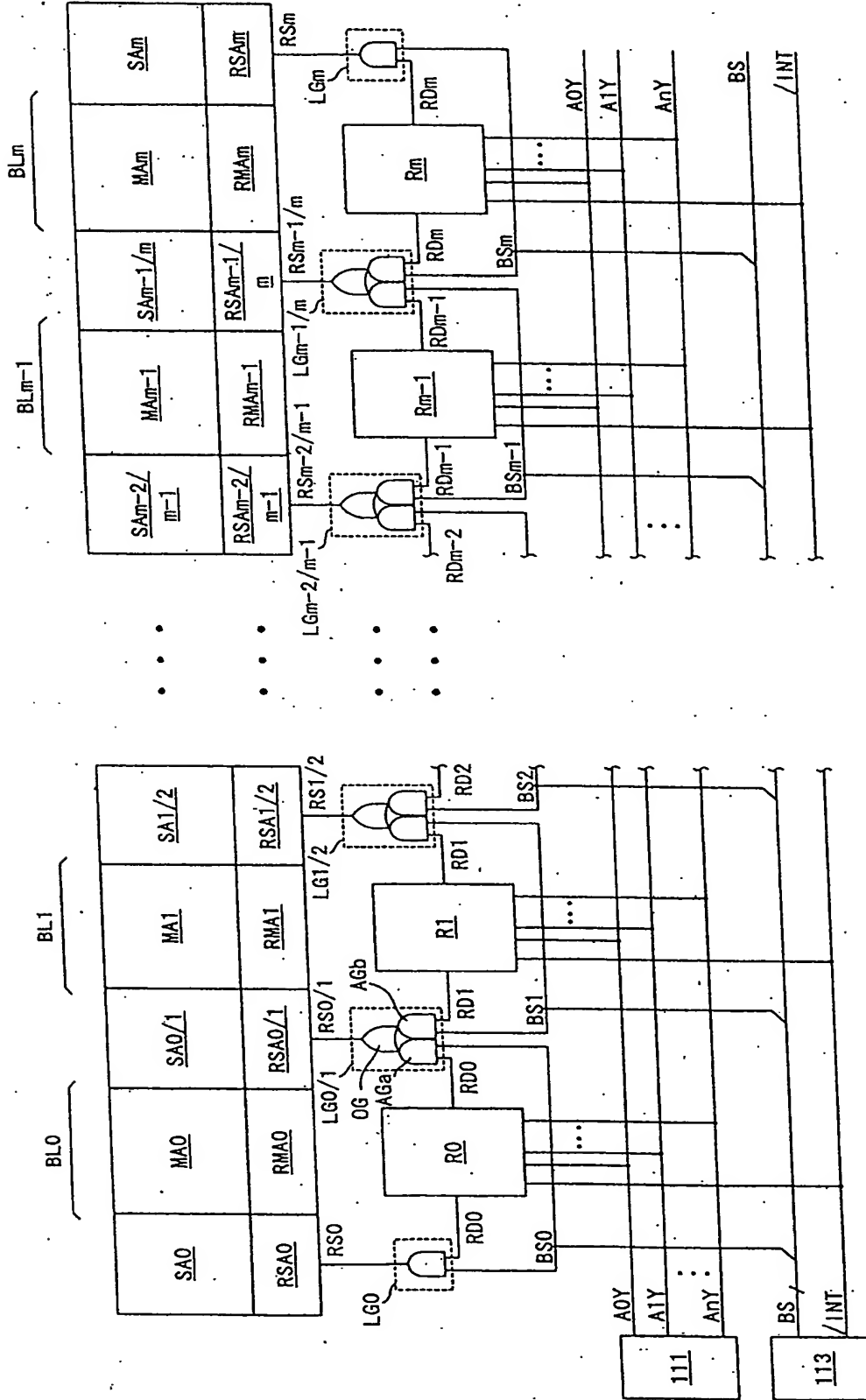


Fig. 1

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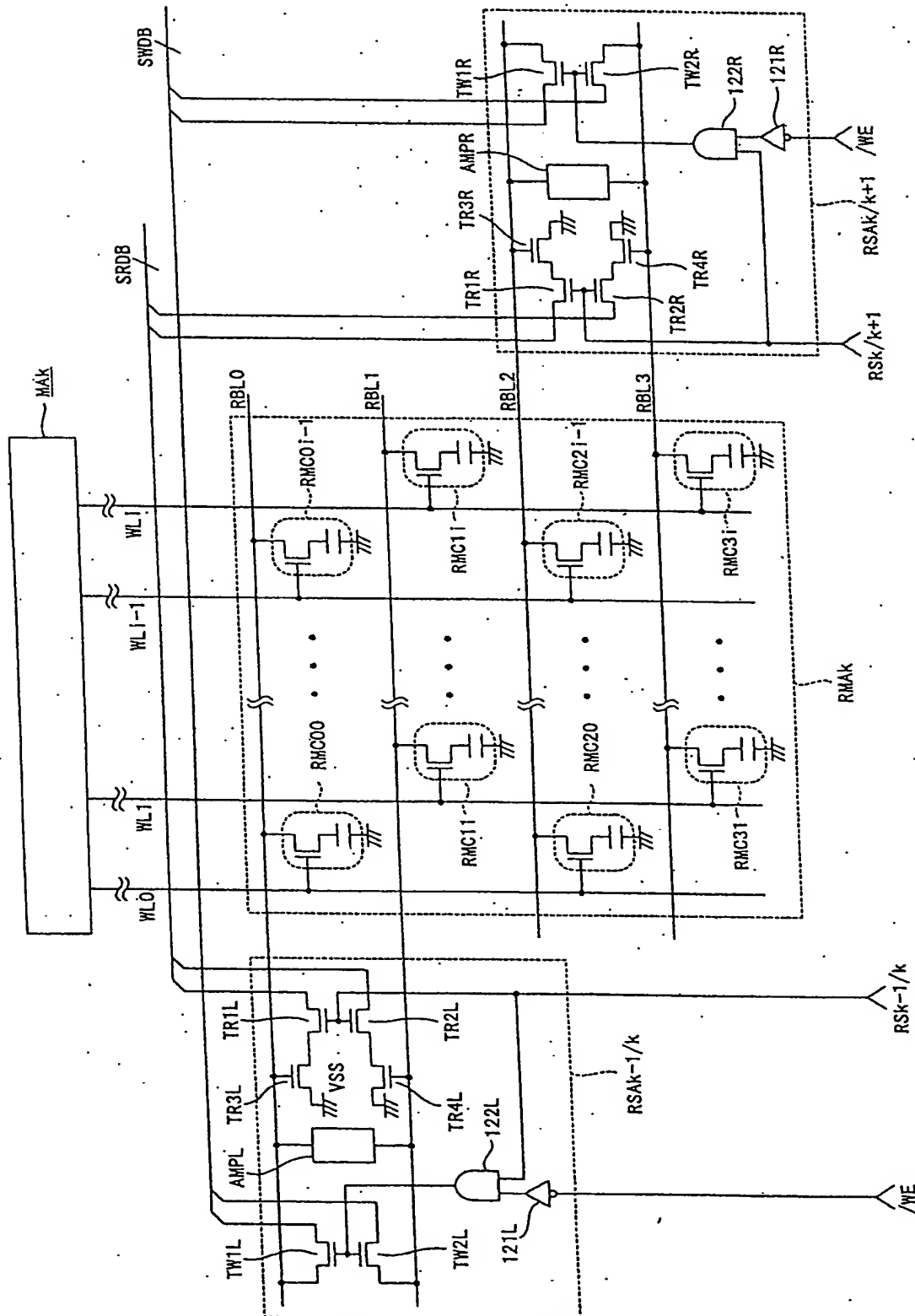


Fig. 2

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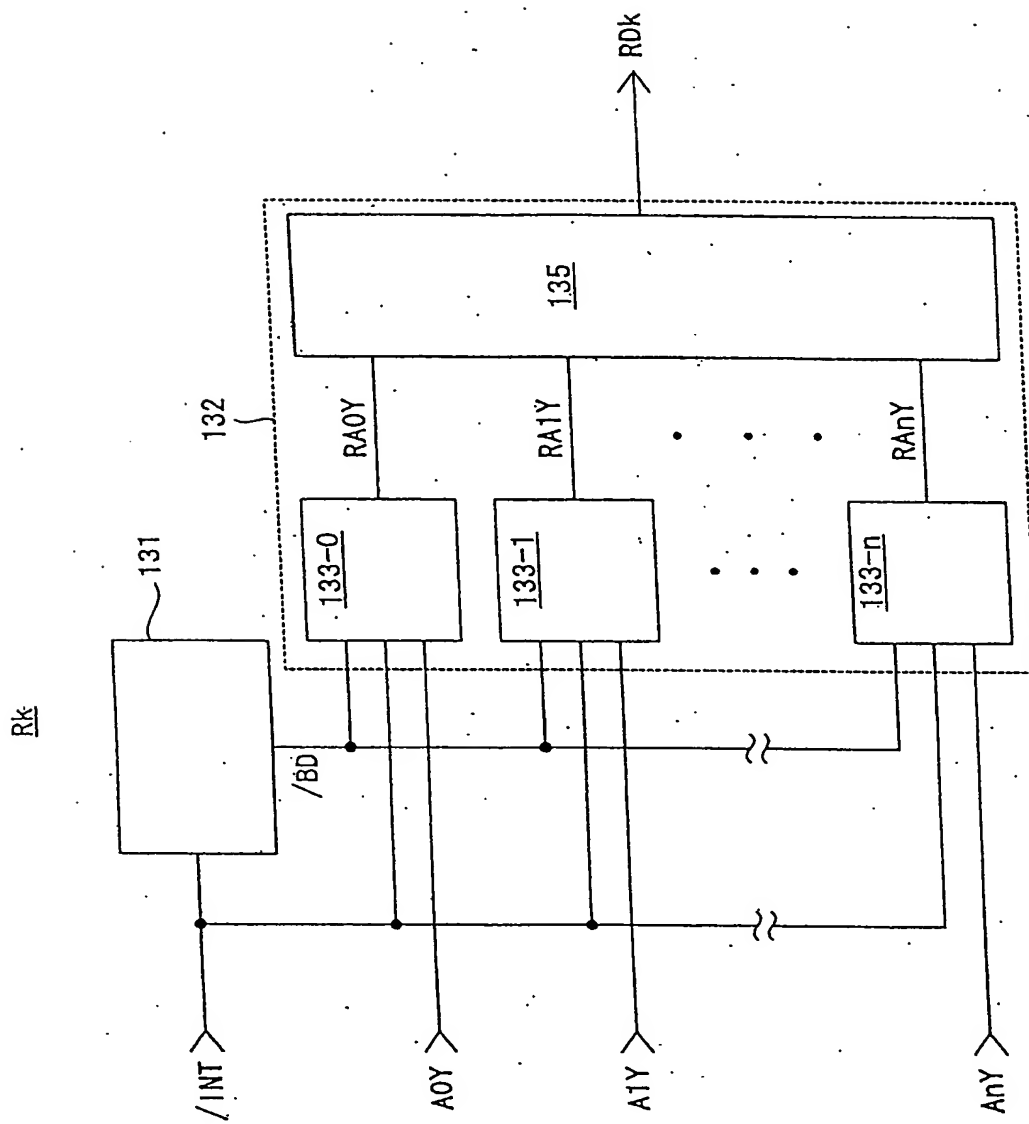
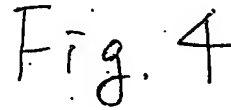


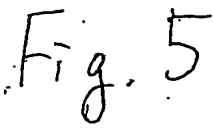
Fig. 3

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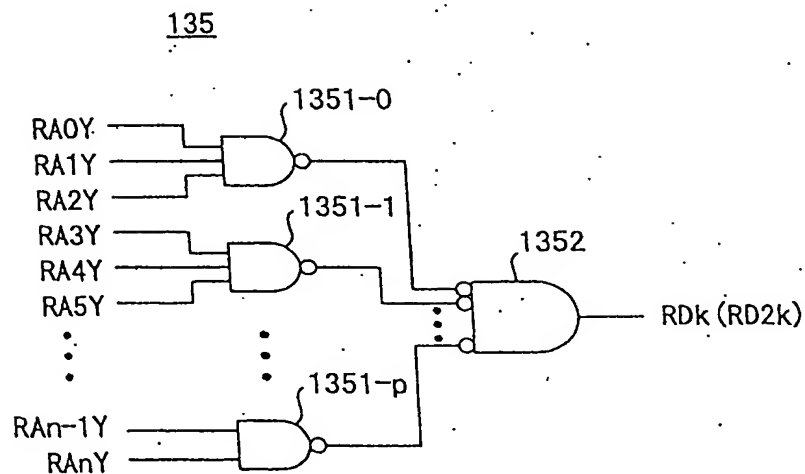


Fig. 6

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Figure 1 is a block diagram of a multi-input multi-output (MIMO) system. The system is organized into two main processing paths, each receiving multiple inputs and producing multiple outputs.

**Inputs:**

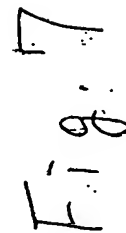
- Top path inputs:  $S_{Am-2}/m-1$ ,  $M_{Am-1}$ , and  $S_{Am-1}/m$ .
- Bottom path inputs:  $R_{S_{Am-2}/m-1}$ ,  $R_{M_{Am-1}}$ , and  $R_{S_{Am-1}/m}$ .

**Processing Blocks:**

- Each path contains two main processing blocks:  $R_{2m-1}$  and  $R_{2m}$ .
- The top path also includes a block labeled  $BSm$  between the two  $R$  blocks.
- The bottom path also includes a block labeled  $BSm$  between the two  $R$  blocks.

**Outputs:**

- Top path outputs:  $A_{0Y}$ ,  $A_{1Y}$ , and  $A_{nY}$ .
- Bottom path outputs:  $B_{0Y}$ ,  $B_{1Y}$ , and  $B_{nY}$ .
- Final system outputs:  $BS$  and  $/INT$ .

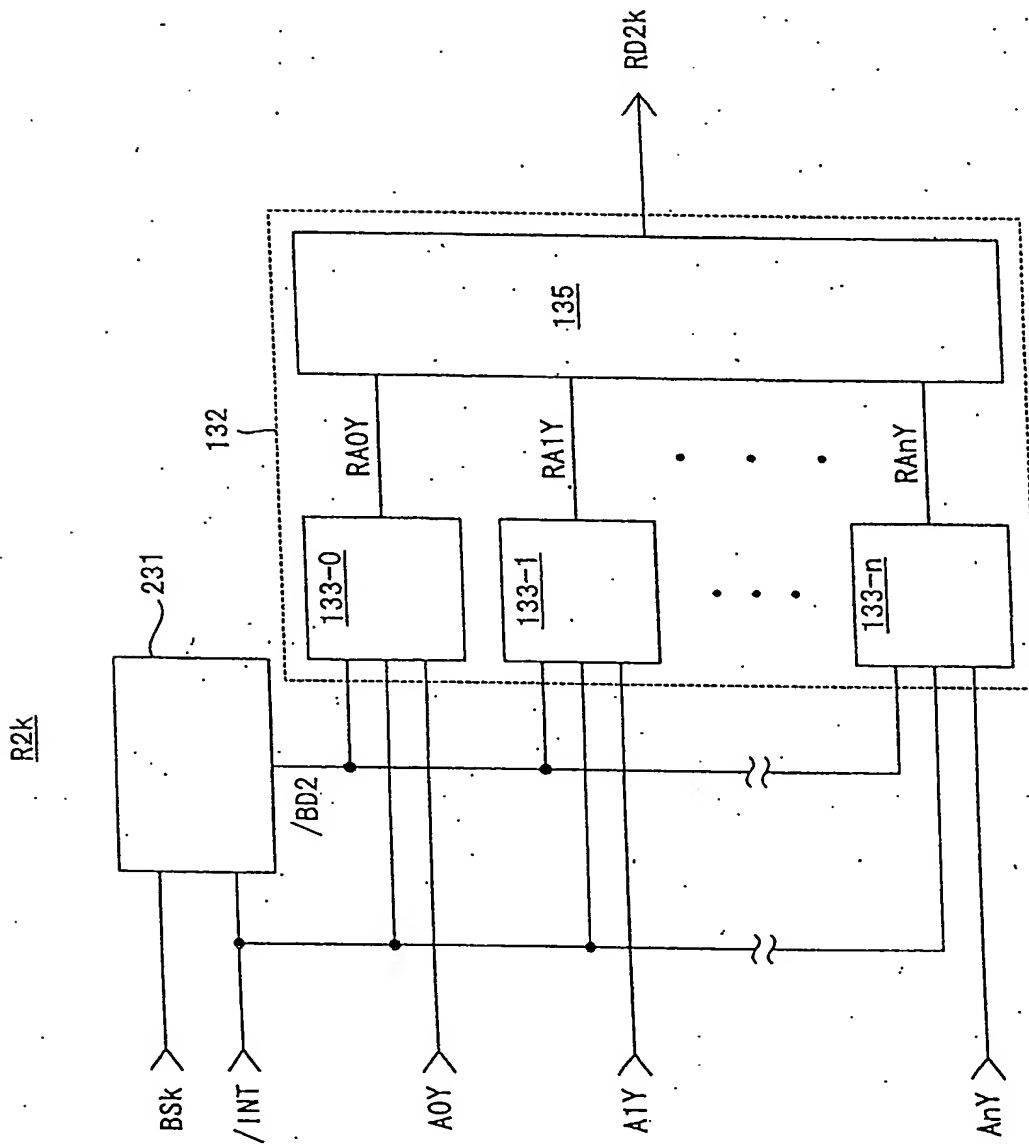


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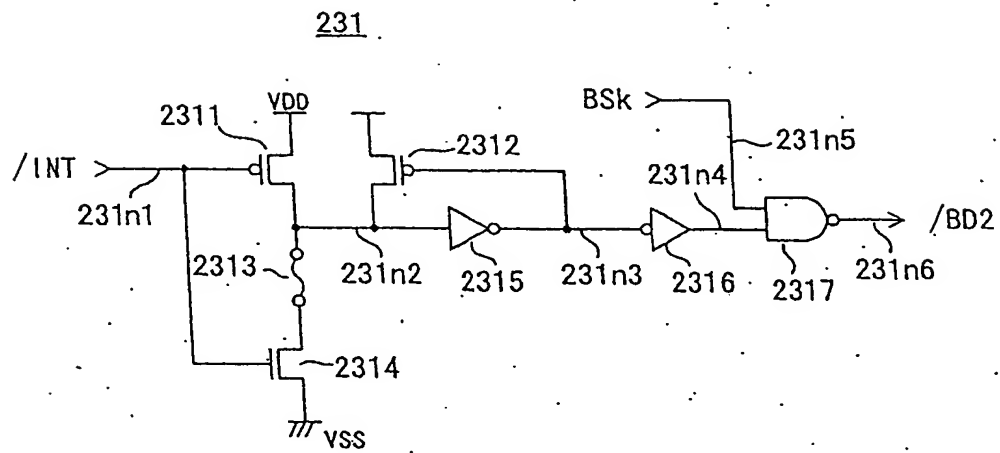


Fig. 9